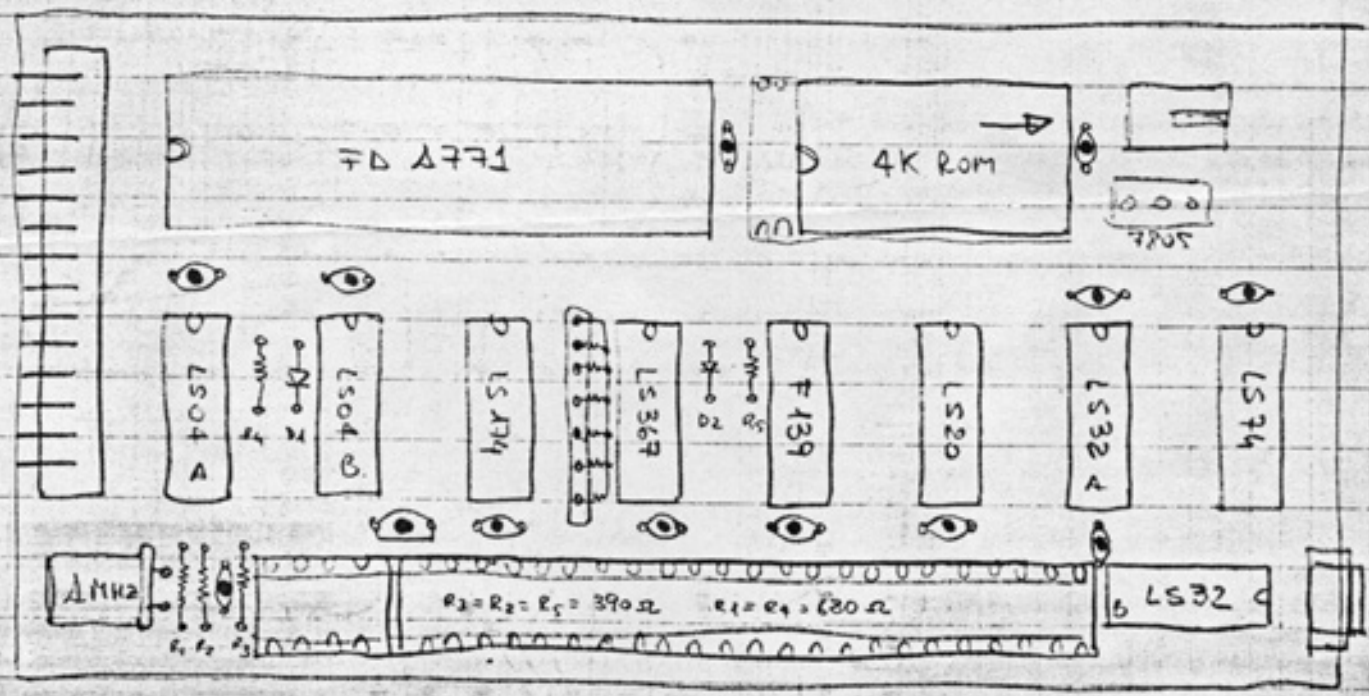
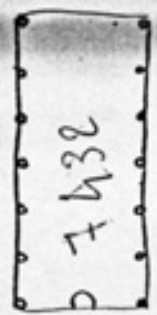
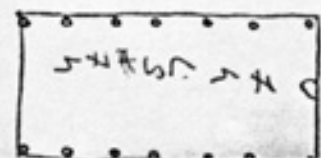
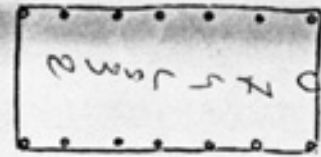
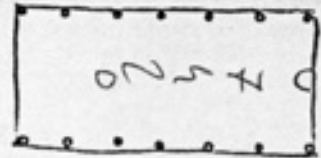
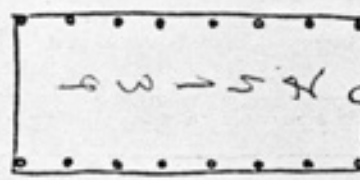
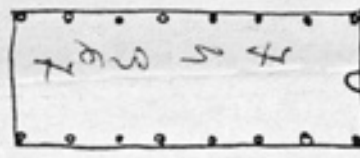
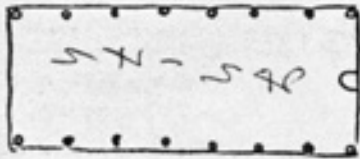
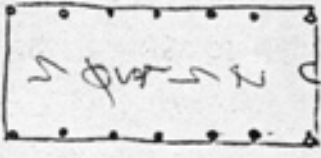
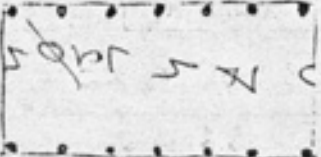
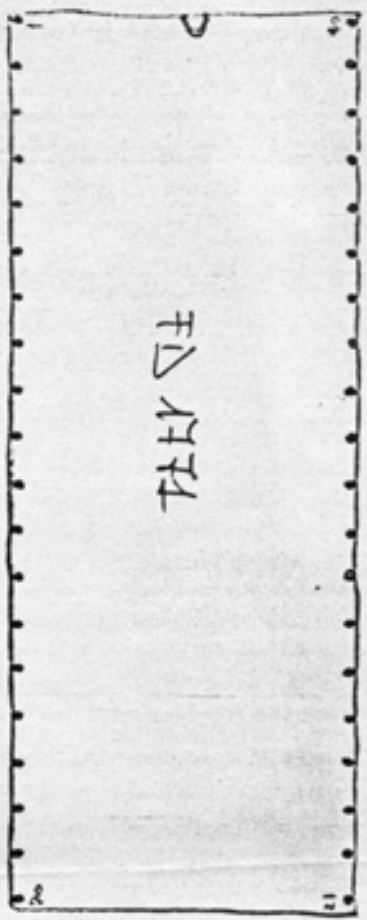


VOLUME 10

- | | | |
|----------|-----|----------------------|
| 74 1771 | x 1 | = 0,47 μF 100V |
| ROM 4K | x 1 | = 0,1 μF 100V |
| 74 LS32 | x 2 | R Pick = 6 x 2,2 |
| 74 LS04 | x 2 | D1 = D2 = 1N4148 |
| 74 LS174 | x 1 | QUARTZ 1 MHz |
| 74 LS367 | x 1 | R1 = R4 = 680 Ω |
| 74 LS20 | x 1 | R2 = R3 = R5 = 390 Ω |
| 74 F139 | x 1 | |
| 74 LS74 | x 1 | |





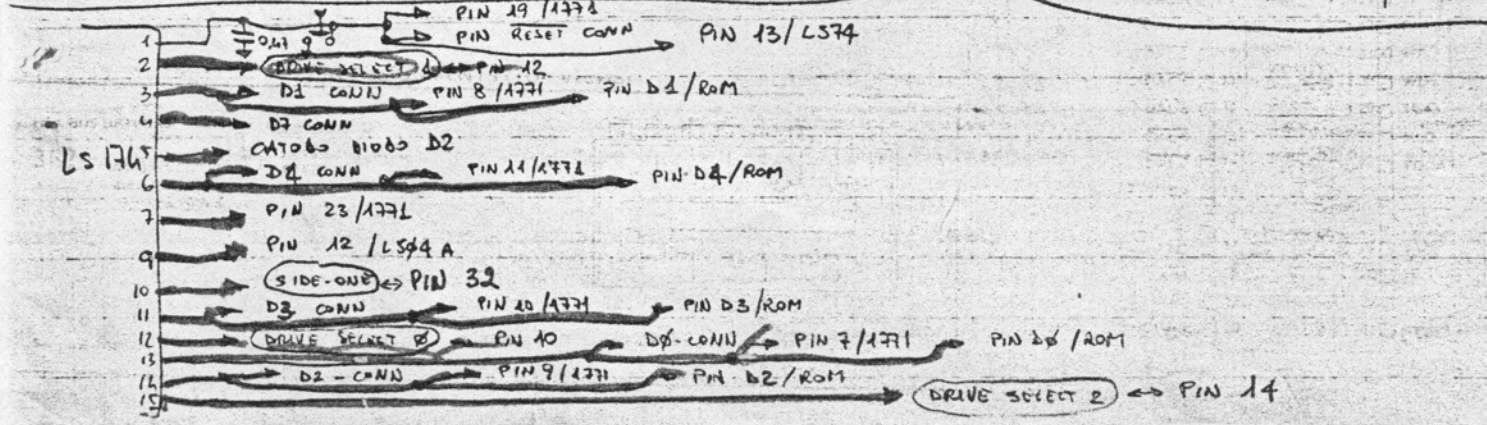
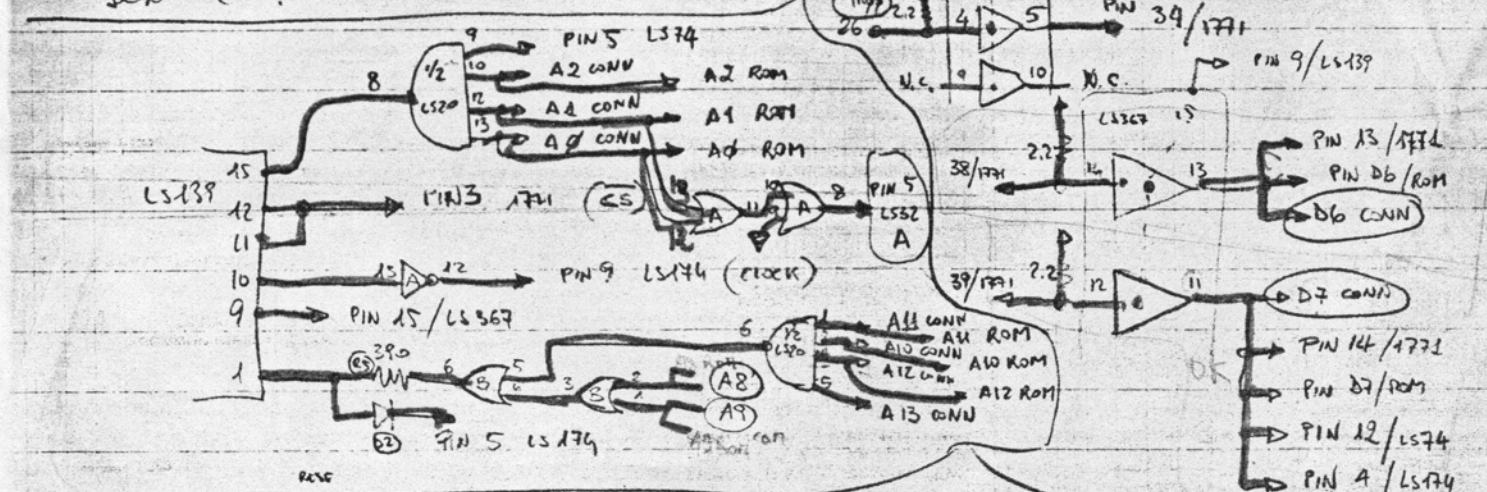
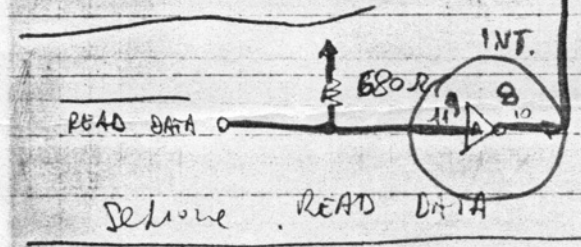
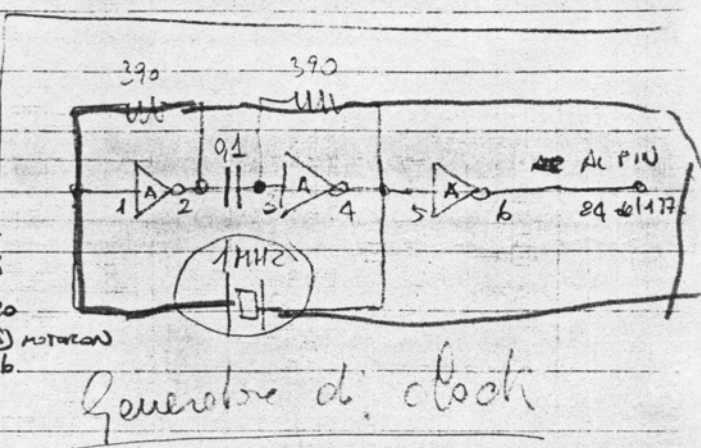
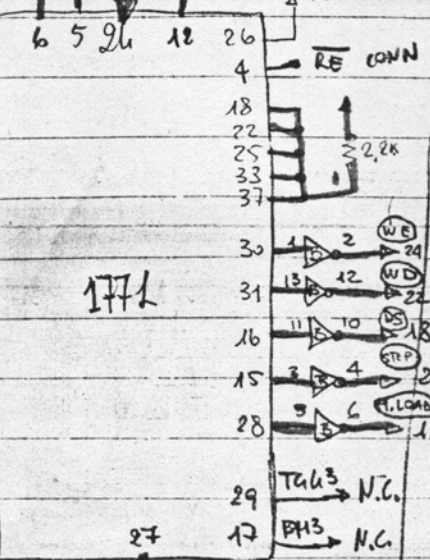
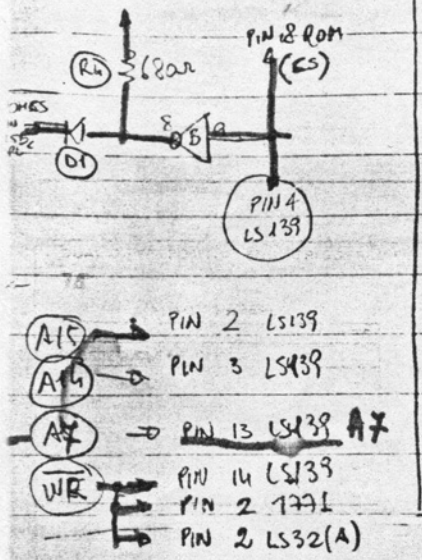
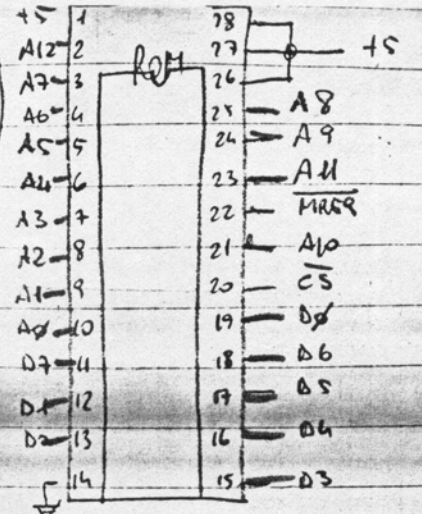
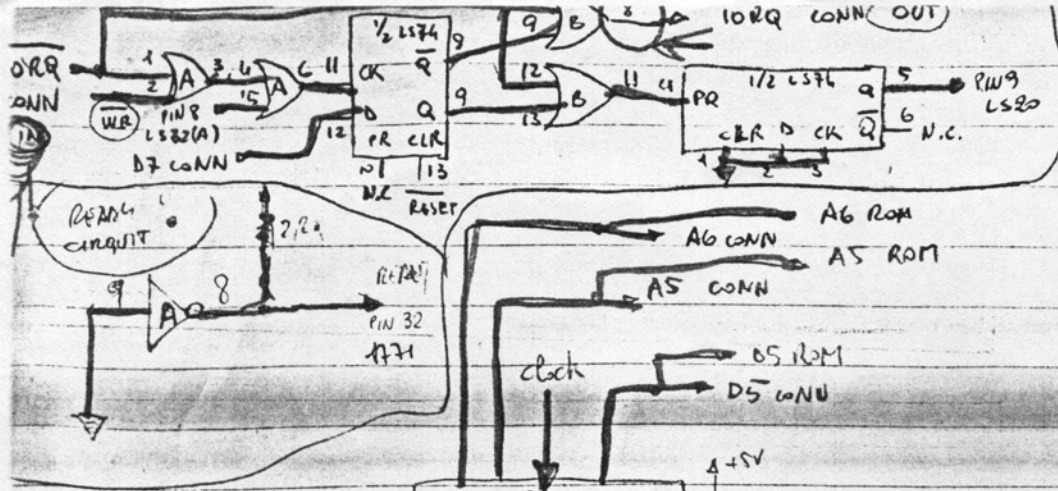
1	2	3	4	5	6	7	8	9	10	11	12
13	14	15	16	17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32	33	34	35	36
37	38	39	40	41	42	43	44	45	46	47	48

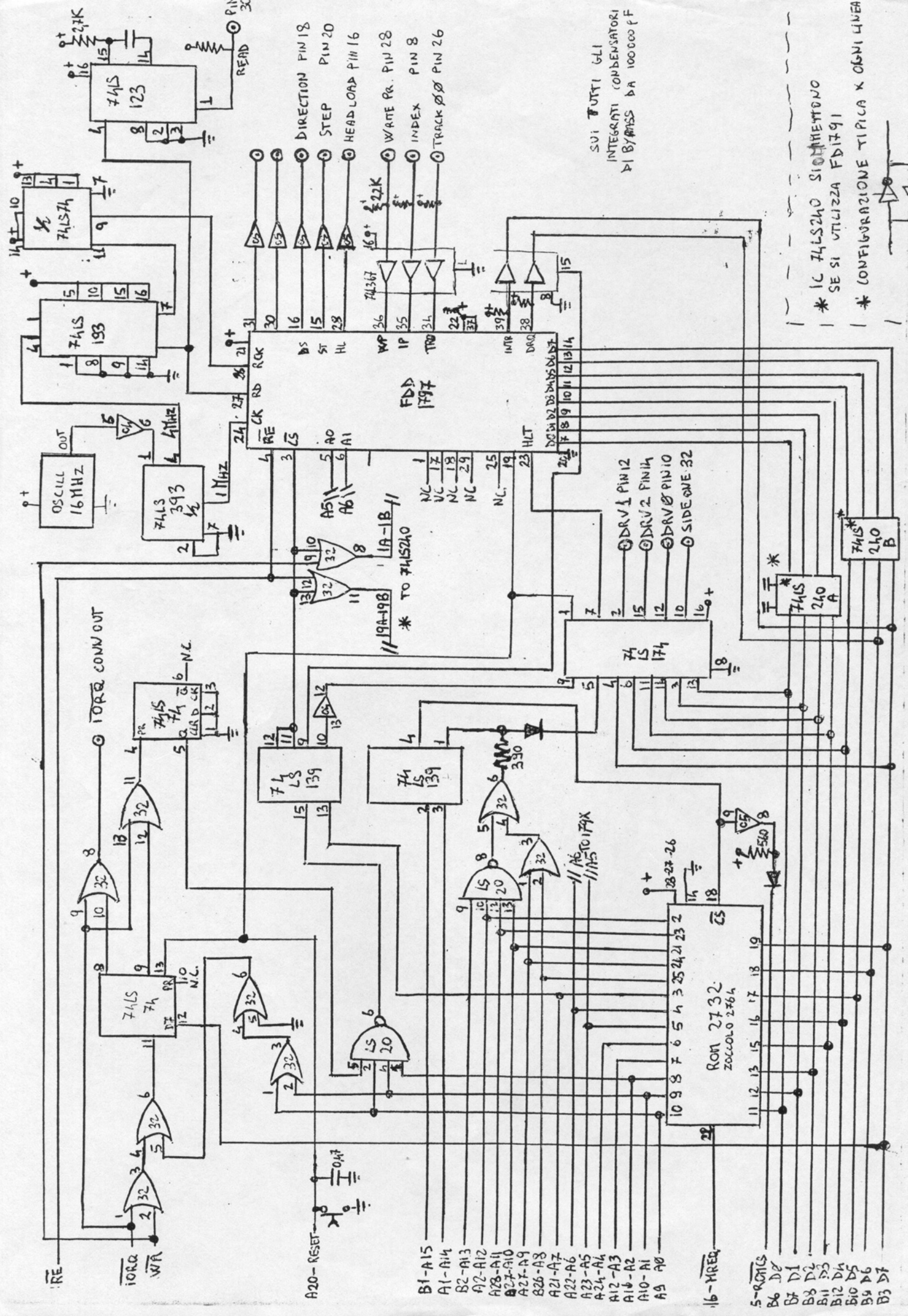
DO-D2 OK
WR OK

CD	1	1	0	0	1	1	0	1	0	1
7F	0	0	0	0	1	1	1	1	1	1
8E	0	1	0	0	0	1	1	1	1	0

0 1 1 2 1 3 / 4 1 5 1 5 1 2 1

LATO INTEGRATI e COMPONENTI



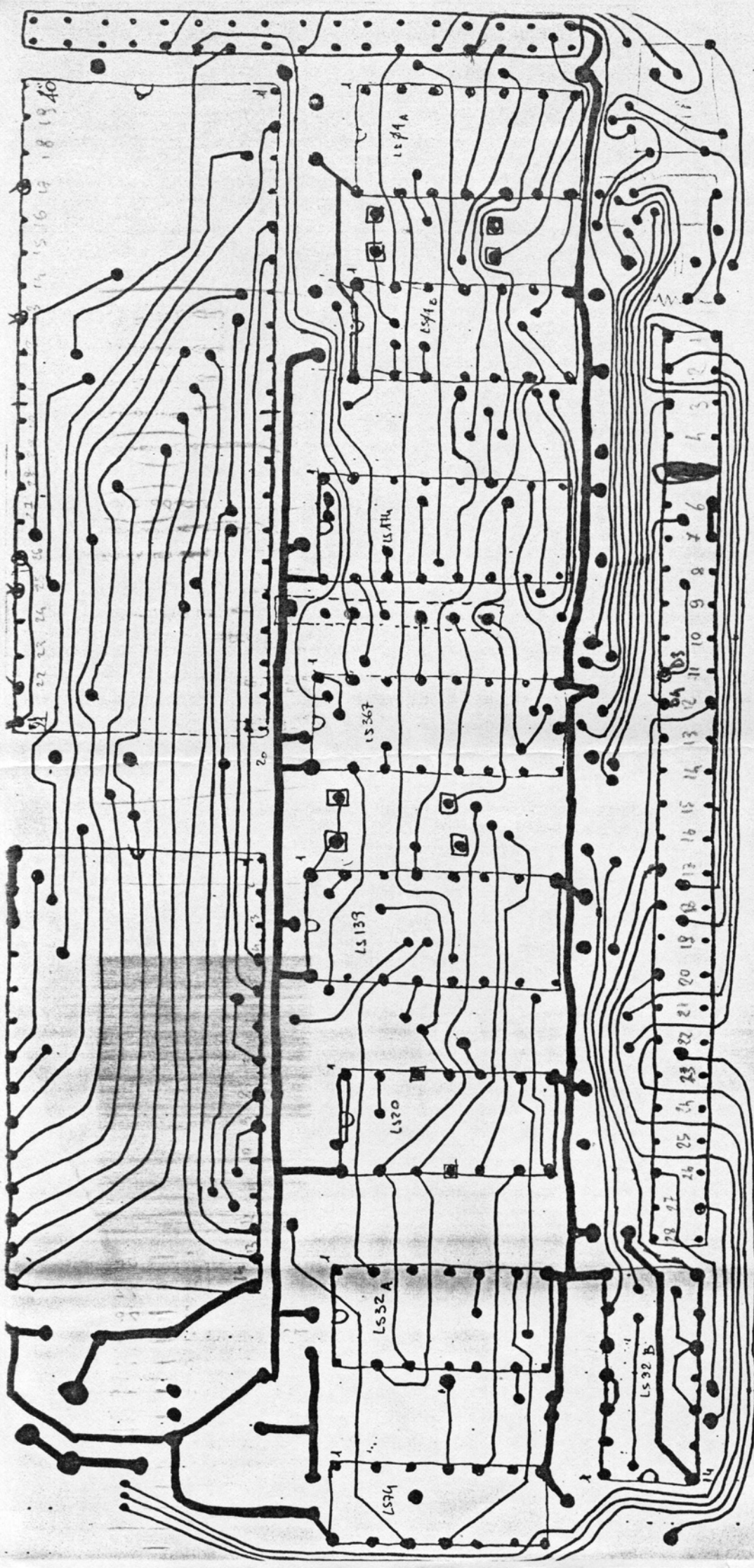


SUI PULSI GLI
INTEGRATI CONDENSATORI
PI BYPASS DA 100000 P.F

* IC 74LS240 SOSTITUIREMO
SE SI UTILIZZA FD1791
* CONFIGURAZIONE TIPICA X OGNI LINEA



- B1-A15
- A1-A14
- B2-A13
- A2-A12
- B2B-A11
- A2F-A9
- B2B-A8
- A21-A7
- A22-A6
- A23-A5
- A24-A4
- A12-A3
- A10-A1
- A9 A0
- 16-MREQ
- 5-RQ1CS
- B6 DE
- B7 D1
- B8 D2
- B11 D3
- B12 D4
- B10 D5
- B4 D6
- B3 D7

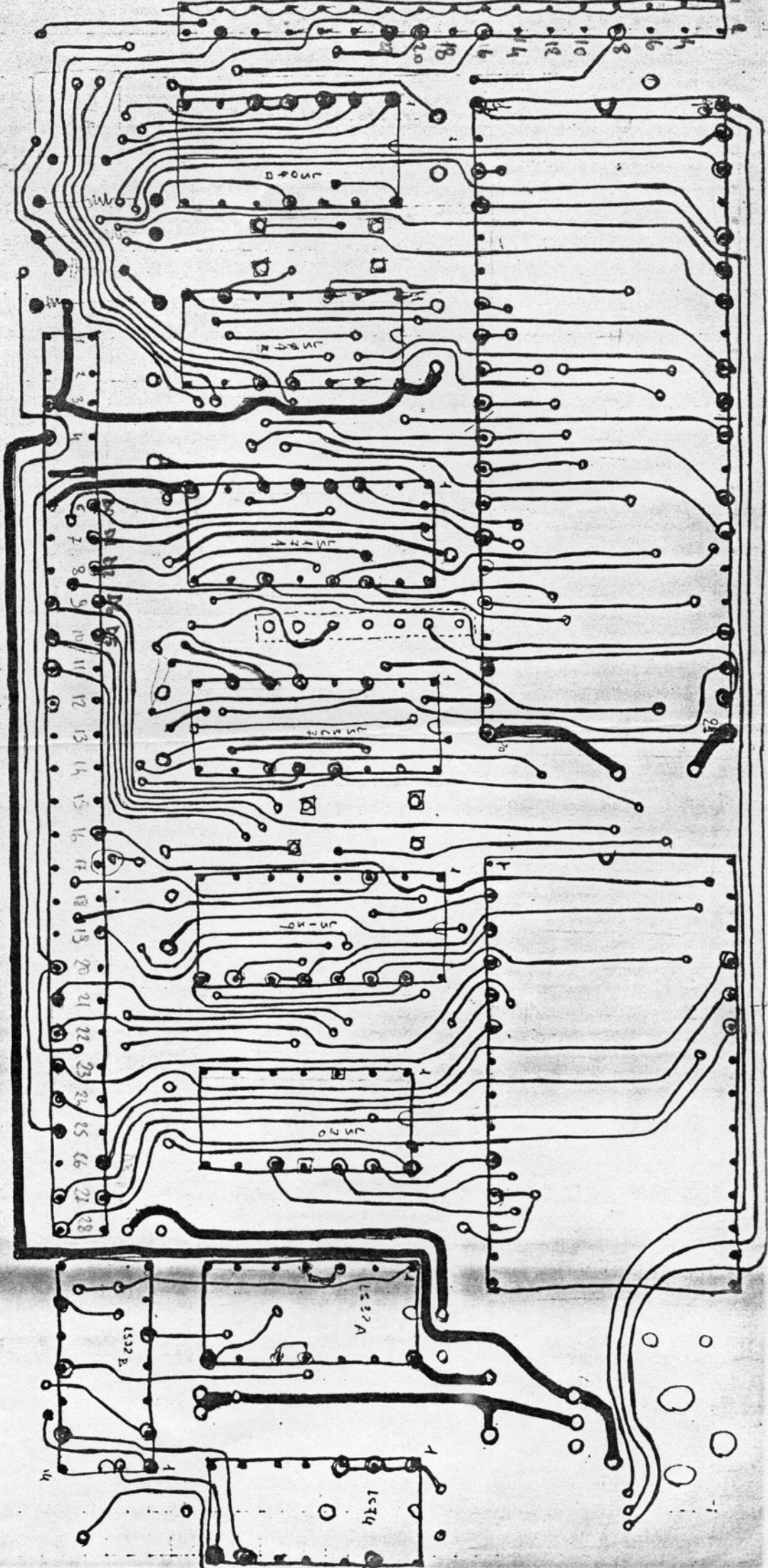


LATO SALDATORE

OK W/L

OK v1
OK v2
BK v3

A0 A1 A2 A3



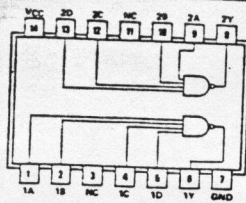
LATO INTEGRATI e COMPONENTI

DUAL 4-INPUT POSITIVE-NAND GATES

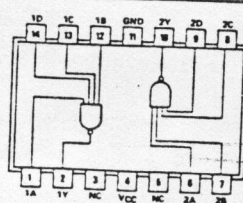
20

positive logic:
Y = ABCD

See page 6-2



- SN5420 (J)
- SN54H20 (J)
- SN54L20 (J)
- SN54LS20 (J, W)
- SN54S20 (J, W)
- SN7420 (J, N)
- SN74H20 (J, N)
- SN74L20 (J, N)
- SN74LS20 (J, N)
- SN74S20 (J, N)



- SN5420 (W)
- SN54H20 (W)
- SN54L20 (T)

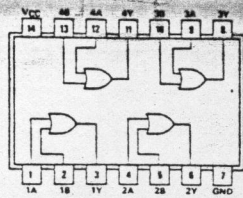
NC—No internal connection

QUADRUPLE 2-INPUT POSITIVE-OR GATES

32

positive logic:
Y = A+B

See page 6-28



- SN5432 (J, W)
- SN54LS32 (J, W)
- SN54S32 (J, W)
- SN7432 (J, N)
- SN74LS32 (J, N)
- SN74S32 (J, N)

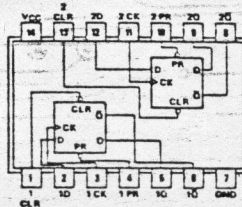
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

74

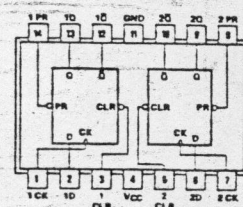
FUNCTION TABLE

INPUTS		OUTPUTS	
PRESET	CLEAR	D	Q
L	H	X	X
L	L	X	X
L	L	X	H*
H	H	↑	H
H	H	↑	L
H	H	L	X
			Q ₀

See pages 6-46, 6-50, 6-54, and 6-56



- SN5474 (J)
- SN54H74 (J)
- SN54L74 (J)
- SN54LS74A (J, W)
- SN54S74 (J, W)
- SN7474 (J, N)
- SN74H74 (J, N)
- SN74L74 (J, N)
- SN74LS74A (J, N)
- SN74S74 (J, N)
- SN5474 (W)
- SN54H74 (W)
- SN54L74 (T)

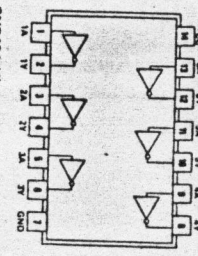


See page 6-2

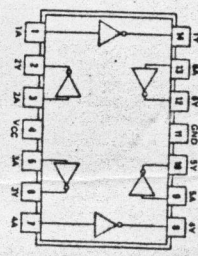
positive logic:
Y = A

HEX INVERTERS

- SN5404 (J)
- SN54H04 (J)
- SN54L04 (J)
- SN54LS04 (J, W)
- SN54S04 (J, W)
- SN7404 (J, N)
- SN74H04 (J, N)
- SN74L04 (J, N)
- SN74LS04 (J, N)
- SN74S04 (J, N)



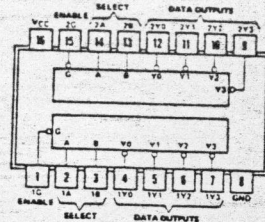
- SN5404 (W)
- SN54H04 (W)
- SN54L04 (T)



DUAL 2-TO-4 LINE DECODERS/MULTIPLEXERS

139

See page 7-134



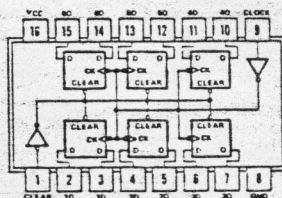
- SN54LS139 (J, W)
- SN54S139 (J, W)
- SN74LS139 (J, N)
- SN74S139 (J, N)

HEX D-TYPE FLIP-FLOPS

174

SINGLE RAIL OUTPUTS
COMMON DIRECT CLEAR

See page 7-253



- SN54174 (J, W)
- SN54LS174 (J, W)
- SN54S174 (J, W)
- SN74174 (J, N)
- SN74LS174 (J, N)
- SN74S174 (J, N)

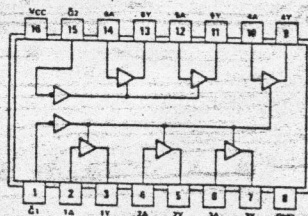
PIN ASSIGNMENTS (TOP VIEWS)

HEX BUS DRIVERS

367

NONINVERTED DATA OUTPUT
4-LINE AND 2-LINE ENABLE INPUTS
3-STATE OUTPUTS

See page 6-36



- SN54367A (J, W)
- SN54LS367A (J, W)
- SN74367A (J, N)
- SN74LS367A (J, N)

